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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 May 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,4,5,7,8,10,12,13,16,18 and 19</u> is/are pending in the application.

4a) Of the above claim(s) <u>21-27</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,4,5,7,8,10,12,13,16,18 and 19</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>09 November 2005</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 were rejected in the Office Action of 21 July 2006. Applicants' response of 20 October 2006 has amended claims 1, 10, 13, 16, and 19. Claims 21-27 are withdrawn. Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are pending in this application.

Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are rejected.

Restriction/Election

1.   Claims 21-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8 May 2006.

Claim Objections

The previous objections to the claims have been withdrawn.

Claim Rejections - 35 USC § 112

Any previous rejections not set forth below have been withdrawn.

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2.   Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. § 112, first

paragraph, as failing to comply with the written description requirement. The claim(s) contains

subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention.

Independent claims 1, 10, and 16 recite a "black box circuit" or "black box circuit model"

in several instances. There appears to be no support for a "black box circuit" or "black box

circuit model" in the application as originally filed.

Claims rejected but not specifically mentioned stand rejected by virtue of their

dependence.

In response, Applicants argue primarily that:

> Applicants respectfully submit that the language "black box circuit" in the above referenced claims is
> inherently implied in Applicants' specification (see para 11, 57, 80, and 89), because "the internals of the
> specific circuit are hidden from the user" is inherently a black box circuit. The Random House Unabridged
> Dictionary ©2006 defines black box as "any unit that forms part of an electronic circuit that has its
> function, but not its components, specified", The American Heritage® Dictionary of the English Language,
> Fourth Edition Copyright © 2000 defines black box as "a device or theoretical construct with known or
> specified performance characteristics but unknown or unspecified constituents and means of operation",
> and finally, The Free On-Line Dictionary of Computer, © 1993-2005 Denis Howe, defines black box as
> "an abstraction of a device or system in which only its externally visible behavior is considered and not its
> implementation or 'inner workings'".

The Examiner respectfully traverses this argument as follows.

Applicants' disclosure states:

> Referring to FIG. 7, the simulator module 26 is a compiled group of function calls to the OS and machine
> instructions. The calls made to simulator module 26 as part of constructing a circuit to be simulated can be
> instantiated and packaged (compiled) together to form code module 25. An interface is added code module
> 25 to form an isolated circuit code module 25. **This code module 25 can then be compiled, producing a
> binary (thus 'hidden') code module.** (Paragraph 80, emphasis added)

Applicants' disclosure states:

> Only the circuit library team needs to know the detailed circuit topology in order to create the source code (in the simulator API language) for each of these functions. **Since this library module is a binary (machine coded) file, the internals of the specific circuit are hidden from the user.** (Paragraph 89, emphasis added)

Applicants' disclosure teaches that a "binary (machine coded) file" hides the internals of the specific circuit from the user. None of the dictionary definitions cited by Applicants makes any reference to compiling to form a binary file. Applicants' reliance upon the <u>extrinsic evidence</u>, which was not included in the original application as filed, would <u>broaden the scope</u> of the claimed invention. Therefore, the claimed invention is not described by the application as originally filed.

The Examiner respectfully suggests that Applicants employ claim language that finds specific support in the application as originally filed. An invention which is "inherently implied" by the disclosure does not comply with the requirements of 35 U.S.C. § 112, first paragraph.

3.   Claims 13 and 19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 13 recites, "wherein said step of assigning said parameters to said code module comprises the step of **the interface providing a call-back function which reflects a predetermined load-modeling.**" (emphasis added)

In contrast, the specification teaches:

> The interface call prototype would reflect the choice of load-modeling as the load is an input into the circuit module. The call-back function allows for the user or calling program to represent the load in whatever

> manner it sees fit, a very useful feature when one thinks of embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. **The invention does not provide for the call-back function (the user does),** but rather the prototype(s) of the call-back(s) function and sufficient documentation to further explain it. Also, the invention could potentially have more than one call-back interface (prototype). (paragraph 87, emphasis added)

Therefore, the claimed subject matter wherein the interface provides a call-back function is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 19 is rejected for similar rationale.

4.   Claims 1, 4-5, 7-8, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. § 112, first paragraph, because the specification, while being enabling for "compiling a code module" (specification, paragraph 80), does not reasonably provide enablement for the broader term "black box circuit". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention commensurate in scope with these claims. To further support this conclusion, Applicants' admission in the response filed on 20 October 2006 states:

> Applicants respectfully submit that the language "black box circuit" in the above referenced claims is inherently implied in Applicants' specification (see para 11, 57, 80, and 89), because "the internals of the specific circuit are hidden from the user" is inherently a black box circuit.

Where a specification "inherently implies" an invention, rather than plainly disclosing the invention, there is necessarily a gap between the disclosure and the claimed invention. In this case, that gap amounts to the difference between the broad term "black box circuit" as claimed and the narrow teaching of "compiling a code module" as described in the specification, paragraph 80. There are certainly other methods by which to achieve a "black box circuit," such

as encryption, remote procedure calls, or some novel and unprecedented method, none of which

are described in the application.

5.   Claims 13 and 19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply

with the enablement requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to enable one skilled in the art to which it pertains, or with

which it is most nearly connected, to make and/or use the invention.

Claims 13 and 19 recite, "wherein said step of assigning said parameters to said code

module comprises the step of **the interface providing a call-back function which reflects a**

predetermined load-modeling." (emphasis added)

In contrast, the specification teaches:

> The interface call prototype would reflect the choice of load-modeling as the load is an input into the circuit module. The call-back function allows for the user or calling program to represent the load in whatever manner it sees fit, a very useful feature when one thinks of embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. **The invention does not provide for the call-back function (the user does)**, but rather the prototype(s) of the call-back(s) function and sufficient documentation to further explain it. Also, the invention could potentially have more than one call-back interface (prototype). (paragraph 87, emphasis added)

Therefore, the specification does not enable one skilled in the art to make and/or use the

invention of claims 13 and 19, but rather expressly discloses an invention that does not possess

the features of claims 13 and 19.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6.   Claims 1, 4-5, 7-8, 10, and 12-13 are rejected under 35 U.S.C. 101 because the claimed

invention is directed to non-statutory subject matter.

Claims 1, 4-5, and 7-8 are directed to "a computerized simulation system" comprising "a

simulator module," "a code module," and "an interface." There is no requirement for any

tangible hardware components in the claim. In light of the specification, which is primarily

directed to computer software, claims 1, 4-5, and 7-8 define a computer *software* "system" and

are therefore nonstatutory as reciting functional descriptive material *per se*. Please see MPEP

2106.

In response, Applicants argue primarily that:

Applicants submit that the claimed invention is statutory because both integrated circuits and the tools that design them are "under the sun" and "made by man". Furthermore, integrated circuits are articles of manufacture, and the simulation system described in Applicants' application and claims 1, 4-5, and 7-8 describes a useful improvement to such circuits. Claims 10 and 12-13 further describe a useful process improvement for integrated circuit design and manufacture.

The Examiner respectfully traverses this argument as follows.

Applicants have not claimed an integrated circuit. The "simulation system" of claims 1,

4-5, and 7-8 is defined broadly enough to encompass computer software *without* a tangible

embodiment. These claims are nonstatutory. Applicants' arguments have been fully considered

but have been found unpersuasive.

Applicants further argue that:

Since Applicants' claim 1 is directed to a simulator comprising components that interact to perform the practical function of simulating a proprietary circuit as a "black box circuit", which further has an interface to receive human input, it is statutory subject matter. The practical result of which is simulation data that induces a user to perform a specific task including but not limited to redesign of the circuit or to provide approval to proceed to manufacturing.

The Examiner respectfully traverses this argument as follows.

Applicants have not claimed "inducing a user to perform a specific task," "redesigning

the circuit," or "providing approval to proceed to manufacturing." Applicants' claim 1 is

directed to a "simulation system" that is defined broadly enough to encompass computer

software *without* a tangible embodiment. These claims are nonstatutory. Applicants' arguments

have been fully considered but have been found unpersuasive.

Applicants further argue that:

> Applicants submit that in the presently claimed invention, a computer program is used in a computerized process where the computer executes the instructions set forth in the computer program to simulate an *integrated circuit* (statutory manufacture) such that the details of the circuit remain hidden to a user. Thus the claimed invention as a whole is a system and process for simulated an integrated circuit using a computer program.

The Examiner respectfully traverses this argument as follows.

Applicants' have not claimed an "integrated circuit." The status of an "integrated circuit"

under 35 U.S.C. § 101 is entirely irrelevant to the invention as claimed. As Applicants' have

stated, in the presently claimed invention *a computer program is used*. Claim 1 makes no

requirement in any fashion for *computer hardware* or *a tangible embodiment for the computer*

program. Therefore, claim 1 is directed to a "simulation system" that is defined broadly enough

to encompass computer software *without* a tangible embodiment. These claims are nonstatutory.

Applicants' arguments have been fully considered but have been found unpersuasive.

Claims 10 and 12-13 define a method that fails to produce a useful, concrete, and tangible

result as established in MPEP 2106(II)(A). Although the recited steps fail to achieve

"modeling," these acts also fail to produce a useful, concrete, and tangible result in isolation. In

light of the specification, which is primarily directed to computer software, the recited steps of

"adding an interface to said code module," and "assigning inputs, outputs, and load parameters,"

etc., define steps of a nonstatutory software method. In order for such a method to meet the requirements of 35 U.S.C. § 101, the method must be limited to a practical application and it must produce a useful, concrete, and tangible result.

In response, Applicants argue primarily that:

> The practical result of [the method of claim 10] is a simulation result that incurs many real world uses including, but not limited to, cost analysis of manufacturing, redesign of the circuit, or approval to proceed to manufacturing.

The Examiner respectfully traverses this argument as follows.

Applicants have not claimed "cost analysis of manufacturing, redesign of the circuit, or approval to proceed to manufacturing." The "useful, concrete and tangible result" must be specified in the claims; i.e., it is not sufficient that a claim reads on a practical application disclosed in the specification. In claim 10, it may be inferred from the claim language that the method results in "a simulation." In the context of the claim, including an API, compiling functions, etc., it is at least reasonable that the claim is broad enough to encompass a computer-implemented method that concludes by producing "a simulation." The claim includes no recitation that the simulation is utilized, displayed, stored, transmitted, or in any other respect exists except for a fleeing instant within the computer. This claim does not define a useful, concrete, and tangible result. Applicants' arguments have been fully considered but have been found unpersuasive.

Applicants further argue that:

> The Office Action further stated that the recited steps in claims 10 and 12-13 fail to achieve either "simulating" or "modeling" and that these acts also fail to produce a useful, concrete, and tangible result in isolation (see Office Action pg. 6, item 5).
> Applicants respectfully disagree that the present invention fails to achieve either "simulating" or "modeling" and request clarification as to why Examiner believes the steps fail to achieve "simulating" or "modeling"...

The Examiner responds as follows.

Applicants are correct in noting that claim 10 recites a step of "simulating". This was an oversight on the part of the Examiner. The text of the rejection has been corrected. However, claim 10 does not produce a useful, concrete, and tangible result as explained above, and the claim is therefore nonstatutory. Applicants' arguments have been fully considered but have been found unpersuasive.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claims 1, 5, 7, 10, 12-13, 16, and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,077,304 to Kasuya.

Regarding claim 1, Kasuya discloses:

A simulator module comprising an API [*"The HDL circuit simulator 102 includes an application program interface (API) 110 that enables other programs to control the operation of the HDL circuit simulator 102 through the use of pre-established instructions (actually procedure calls)."* (column 4, lines 7-11)];

wherein said API comprises at least one function [*"procedure calls"* (column 4, lines 7-11)] and wherein said simulator module uses said function to define a component of the black box circuit and its corresponding simulated behavior [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (column 4, lines 25-32)];

And wherein said function is recorded as a recorded function and said recorded function, when called during a simulation, reproduces a behavior corresponding to the black box circuit [*supra* (column 4, lines 25-32)];

A code module which is formed from a compiled plurality of recorded functions, wherein the code module makes calls to the simulator module during simulation of the black box circuit [*"Each test bench is initially prepared as a test bench source file 130, which is then processed by a test bench **compiler** 132 so as to generate an **executable test bench object file.**"* (column 5, lines 3-6); ***"The test bench object file is executed in conjunction with a verification engine 136 that control and coordinates the tasks performed by the circuit verification subsystem 104. A test bench is a computer program, and thus can perform any operation, sequence of operations, and/or combination* [of] *operations, that the circuit verification subsystem 104 is capable of performing."*** (column 5, lines 7-13)]; and

An interface between said code module and a user program wherein a user defines said code module inputs, outputs, and load parameters, and wherein the internals of the black box circuit are hidden from the user [*"The performance of the specified circuit as simulated by the*

simulation engine 112 is also determined by the waveforms of the specified circuit's input signals. The input signal waveforms can be specified by the user via the user interface 114, 115, or can be specified through the API 110 through the use of predefined procedure calls for defining input signal waveforms." (column 4, lines 38-45); note that Kasuya discloses "compiling" the test bench source file (column 5, lines 3-6) which anticipates not only the claim limitation but also the support for this claim limitation in Applicants' specification, paragraph 89].

In response, Applicants argue primarily that:

Kasuya teaches a simulation engine that simulates the operation of the circuit specified by the *HDL circuit specification* and not a black box circuit, which is specified by a plurality of recorded functions which have been compiled into a code module (see Kasuya Col. 4, lines 25-28). The HDL circuit specification defined in Kasuya is not a black box circuit specification. It is a specification including all details of every circuit in the design.

The Examiner respectfully traverses this argument as follows.

The Examiner respectfully requests that Applicants provide citations of the factual evidence thought to support Applicants' conclusory statements. In particular, it is unclear where, in Kasuya, Applicants find support for the conclusions that "The HDL circuit specification defined in Kasuya is not a black box circuit specification. It is a specification including all details of every circuit in the design." There appears to be no such statement in Kasuya.

Kasuya teaches defining a circuit specification through a plurality of recorded function calls [*"the HDL circuit specification 106 received from the system's user via a **user interface procedure 114** that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (column 4, lines 25-32)]. Kasuya further teaches recording a plurality of functions defining a circuit specification [*"The simulation*

engine 112 simulates the operation of the specific circuit components in accordance with

predefined circuit models 116, typically stored in a library of such models." (column 4, lines

32-35)]. It is unclear how Applicants distinguish the claimed invention from the disclosure of

Kasuya based upon the <u>factual evidence found in the Kasuya reference</u> as compared to <u>the claim</u>

<u>language</u>.

      Applicants' arguments have been fully considered but have been found unpersuasive.

      Applicants further argue that:

> Furthermore, Kasuya simulates the operation of circuit components in accordance with predefined circuit models, which are typically stored in a library (see Kasuya Col. 4 lines 32-35). Applicants' black box circuit is a plurality of recorded function calls that have been compiled into a functional code module (not a predefined static circuit model). The code module makes calls to the simulator module when a black box circuit model behavior information is needed during simulation (See Applicants' abstract, summary, paragraphs 8-11, 89, 102, Fig. 7, and claims 1, 7, 10, and 16).
>   Therefore, Applicants su7bmit that the 356 U.S.C. § 102 rejection of claim 1 as being anticipated by Kasuya has been overcome because Kasuya fails to anticipate all of the elements of claim 1...

The Examiner respectfully traverses this argument as follows.

      Applicants' argument appears to lack a clear conclusion. It is unclear where Applicants

find support in Kasuya for the reference to a "predefined static circuit model." Further,

assuming *arguendo* that such evidence is found in Kasuya, the claimed invention is directed to

<u>recording</u> functions that define a circuit. It is unclear how *<u>recorded</u>* functions could be regarded

as anything but *<u>predefined and static</u>*.

      The Examiner respectfully submits that the claimed "code module" formed from a

plurality of recorded functions appears consistent with a "library".

      Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 5, Kasuya discloses that the interface between the user program and code module includes a dynamic callback function which defines the load parameters [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (coliumn 4, lines 26-32)].

Regarding claim 7, Kasuya discloses that the code module is compiled into a library [*"Each test bench is initially prepared as a test bench source file 130, which is then processed by a test bench compiler 132 so as to generate an executable test bench object file 134."* (column 5, lines 3-6)].

Claim 10 recites the method performed by the system of claim 1. As Kasuya anticipates the system of claim 1, Kasuya similarly anticipates the method performed by that system.

Claim 12 recites the method corresponding to the system of claim 7. As Kasuya anticipates the system of claim 7, Kasuya similarly anticipates the method performed by that system.

Regarding claim 13, Kasuya discloses that the step of assigning parameters to said code module comprises the step of the interface providing a call-back function which reflects a predetermined load-modeling [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a*

user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)." (coliumn 4, lines 26-32); *"A test bench is a computer program, and thus can perform any operation, sequence of operations, and/or combination of operations, that the circuit verification subsystem 104 is capable of performing."* (column 5, lines 10-15)].

Claim 16 recites a program storage device storing instructions that perform the method of claim 1. As Kasuya anticipates the system of claim 1 and further discloses a computer system [*"In the preferred embodiment, the HDL circuit simulator 102 and the circuit operation verifier 104 are executed by the same CPU 108, and in fact operate together in most respects as a single program. Suitable operating systems 109 include, for example, UNIX [...], Solaris [...], and Windows NT [...]."* (column 3, line 66 – column 4, line 6)], Kasuya similarly anticipates the program storage device storing instructions that perform the method of claim 1.

Claim 18 recites the method corresponding to the system of claim 7. As Kasuya anticipates the system of claim 7, Kasuya similarly anticipates the program storage device storing instructions that perform the method of claim 7.

Regarding claim 19, Kasuya discloses that the step of assigning parameters to said code module comprises the step of the interface providing a call-back function which reflects a predetermined load-modeling [*"The HDL circuit simulator 102 includes a simulation engine 112 that simulates the operation of the circuit specified by the HDL circuit specification 106 received from the system's user via a user interface procedure 114 that handles communications with a user via a computer user interface 115 (hereinafter collectively called the user interface 114, 115)."* (coliumn 4, lines 26-32); *"A test bench is a computer program, and thus can perform any*

operation, sequence of operations, and/or combination of operations, that the circuit verification

subsystem 104 is capable of performing." (column 5, lines 10-15)].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c)

and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

8.   Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kasuya in view

of "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE

100).

Regarding claim 4, Kasuya discloses the invention of claim 1.

Kasuya does not expressly disclose a "static load model".

IEEE 100 discloses a "resistor," described as "An element within a circuit that has a

specified resistance value designed to restrict the flow of current," i.e. a *static load*.

Kasuya and IEEE 100 are analogous art because both are directed to electrical

engineering.

At the time of the invention, it would have been obvious to a person of ordinary skill in

the art to include a *static load* model, for example, a *resistor*, in the circuit simulation system of

Kasuya.

The motivation for doing so would have been found in the knowledge of a person of

ordinary skill in the art in recognition of the fact that a resistor is a basic and fundamental

electrical component that is necessary for the design of almost every useful electrical device.

Therefore, it would have been obvious to combine IEEE 100 with Kasuya to obtain the

invention as specified in claim 4.

9.   Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kasuya in view

of "Microsoft Computer Dictionary, Fifth Edition" (Microsoft Computer Dictionary).

Regarding claim 8, Kasuya discloses the invention of claim 7.

Kasuya does not expressly disclose that the code module comprises a "dynamically loadable library".

Microsoft Computer Dictionary discloses a "dynamic-link library," described as "A feature of the Microsoft Windows family of operating systems and OS/2 that allows executable routines to be stored separately as files with DLL extensions and to be loaded only when needed by a program," i.e. a *dynamically loadable library*.

Kasuya and Microsoft Computer Dictionary are analogous art because both are directed to computer software.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a *dynamically loadable library*, for example, a *dynamic-link library*, in the circuit simulation system of Kasuya.

The motivation for doing so would have been found in the knowledge of a person of ordinary skill in the art in recognition of the fact that a DLL is a standard part of the ubiquitous Microsoft Windows operating system and provides the flexibility innate in storing executable routines in separate files.

Therefore, it would have been obvious to combine Microsoft Computer Dictionary with Kasuya to obtain the invention specified in claim 8.

In response to the rejections above under 35 U.S.C. § 103(a), Applicants argue primarily that:

> Since there is no teaching, motivation, or suggestion in any of the cited references to combine the teachings of Kasuya with the IEEE, Microsoft, and White references, one of ordinary skill in the art would not have been motivated to create a code module from compiled recorded function calls, such that the code module has the ability to simulate a black box circuit whose circuit details are hidden from the user.

The Examiner respectfully traverses this argument as follows.

Motivation has been expressly described in the rejections above. Applicants' arguments have been fully considered but have been found unpersuasive.

Additionally, Applicants may be interested in reviewing *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 80 USPQ2d 1641 (Fed. Cir. 2006).

Applicants further argue that:

> Furthermore, the White, IEEE, and Microsoft references show only fundamental electronic principles and rudimentary software programming techniques and would not have provided one of ordinary skill in the art at the time of the invention with the enablement to make and practice the invention.

The Examiner respectfully traverses this argument as follows.

Applicants conclusory statements are not supported by a showing of facts. Applicants' arguments have been fully considered but have been found unpersuasive.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.
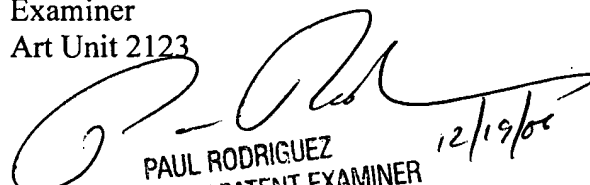
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
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12/19/06